19. (Amended) The switched network system according to claim 17, wherein the plurality of programmable system settings include a port operation code, and the scheduler sets the operation of the port based on the port operation code.

21. (Amended) The switched network system according to claim 17, wherein the plurality of programmable system settings include a sequence of an N number of memory access slot assignments that is continuously repeated by the scheduler in assigning memory access slots.

22. (Amended) The switched network system according to claim 21, wherein the plurality of programmable system settings include a wrap-around bit at an end of the sequence and the scheduler returns to a first memory access slot at a start of the sequence upon detecting the wrap-around bit.

23. (Amended) The switched network system according to claim 18, wherein the memory access slot assignment table memory is a RAM.

24. (Amended) The switched network system according to claim 18, wherein the memory access slot assignment table memory is a group of registers.

REMARKS

In response to the Office Action dated September 11, 2002, claims 4, 13, 15, 17, 18, 19 and 21-24 are amended. Claims 1-25 are now active in this application. No new matter has been added.

The indication that claims 5, 7, 13-15, 20 and 22 would be allowable if rewritten to overcome the rejections under 35 U.S.C. §112, second paragraph, set forth in this office action and to include all of the limitations of the base claim and any intervening claims is acknowledged and appreciated.

Formal drawings are submitted concurrently herewith.

REJECTION OF CLAIMS UNDER 35 U.S.C. § 112, SECOND PARAGRAPH

Claims 4, 5 and 11-25 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

Claims 5, 14, 16, 18, 20 and 23-25 are rejected under 35 U.S.C. §112, second paragraph because they depend from rejected claims 4, 11 and 17, respectively.

In support of the rejection of claims 4, 5 and 11-25, the Examiner identifies phrases that are deemed to be confusing and/or lack clear antecedent basis. By this response, nist of the noted points of indefiniteness have been appropriately addressed, and the claims are believed to recite the invention with the degree of precision and particularity required by the statute.

However the objection to "a memory" recited in line 4 of claim 11 and "the memory" recited in line 4 of claim 17, as being unclear is respectfully traversed.

Case law precedent has established that an analysis under 35 U.S.C. § 112 begins with a determination of whether the claims do, in fact, set out and circumscribe a particular area with a reasonable degree of precision and particularity. Claim language is viewed not in a vacuum, but in light of the teachings of the prior art and of the application disclosure as it would be interpreted by one possessing the ordinary level of skill in the art. ***In re Johnson***, 558 F.2d 1008, 194 USPQ 187 (CCPA 1977); ***In re Moore***, 439 F.2d 1232, 169 USPQ 236 (CCPA 1971).

A decision on whether a claim is invalid under this section of the statute requires a determination of whether those skilled in the art would understand what is claimed when the claim is read in light of the specification, ***Seattle Box Co. v Industrial Crating & Packing***, 731 F.2d 381, 385, 221 USPQ 568, 574 (Fed. Cir. 1984).

In determining definiteness, no claim may be read apart from and independent from the disclosure on which it is based. ***In re Cohn***, 169 USPQ 95, 98 (CCPA 1971); ***In re Kroekel***, 183 USPQ 610, 612 (CCPA 1974):

> ... claims are not to be considered in a vacuum, "but always in light of the teachings of the prior art and the particular application disclosure as it would be viewed by one possessing the ordinary level of skill in the pertinent art." When considered in light of the prior art and the specification, claims otherwise indefinite may be found reasonably definite.

The Examiner's question concerning clarity of these recitations results from the fact that the Examiner is reading the claims in a vacuum and not in light of the specification. It is submitted that when the claim language is read in light of the specification, an artisan would readily understand what the metes and bounds of the invention are. More specifically, an artisan would understand "a memory" is different from "an external memory". Consequently, "a memory" recited in claim 11, line 4, and "the memory" recited in claim 12, line 4, are definite when the language is read in light of the specification.

REJECTION OF CLAIMS UNDER 35 U.S.C. § 102 AND § 103

Claims 1, 2, 4 and 11 are rejected under 35 U.S.C. §102(e) as being anticipated by Pei et al. (hereinafter, Pei).

The rejections are respectfully traversed.

The factual determination of lack of novelty under 35 U.S.C. § 102 requires the identical disclosure in a single reference of each element of a claimed invention such that the identically

claimed invention is placed into possession of one having ordinary skill in the art. ***Helifix Ltd. v. Blok-Lok, Ltd.*** 208 F.3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); ***Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.,*** 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994). There is a significant difference between the claimed invention and the arrangement and methodology disclosed by Pei that scotch the factual determination that Pei identically describes the claimed invention.

Claim 1 recites:

> A network switch comprising:
> a plurality of ***ports*** configured for transferring data packets;
> an external memory interface configured for transferring data packets between the network switch and an external memory, the external memory interface including a ***scheduler*** for selectively ***assigning memory access slots of the external memory interface to ports*** based on respective programmable information entries.

Claim 11 recites:

> A method of assigning memory access slots in a network switch to a plurality of network switch ports, each configured for transferring data packets to an external memory, the method comprising:
> storing programmed memory access slot assignment information into a memory; and
> selectively ***assigning memory access slots to the respective network switch ports*** based on the programmed memory access slot assignment information.

The Examiner maintains that Pei discloses an interface for transmitting ATM cells over a link to a node of an ATM network using a programmable cell transmission scheduler which controls scheduling of cells for transmission over the link including a scheduling table which is store in memory, for use by the programmable cell transmission scheduler whereby the scheduling table includes a plurality of lines, each of which contain an index identifying one of a plurality of virtual path connections that may utilize the link and col. 5, lines 3-13 which recite the scheduler

using one or more tables to assign traffic of a variety of types into respective cell transmit time slots ... However, the Examiner has not identified where Pei discloses ***assigning memory access slots of the external memory interface to ports***, so that individual ports can write to and read from the external memory. All the Examiner has established is that scheduler 45 schedules a variety of different types of traffic on a hierarchical basis for a plurality of virtual paths within the ATM link. The scheduler (45) implements a process similar to that of FIG. 1 ***using one or more scheduling tables***. As shown from the flow indicated in FIG. 4 of Pie, the scheduler is used to schedule from the TX FIFO, where cells, presumably from external memory 29, have been placed for transmission. A substantial portion of the description in Pei deals with discussion of the cell transmit time, not with time slots for scheduling access, by each of the plurality of ports of the ATM, to the external memory 29. There is nothing in Pei which discloses or suggests that the disclosed scheduling of ATM cell traffic for ***transmission over an ATM link*** can be used for scheduling (assigning) of memory access slots to the respective ports of the ATM so that data can be written to and read from the external memory. It is even more telling that col. 5, lines 3-13 of Pei, identified by the Examiner, has no description of anything concerning scheduling (assigning) of memory access slots to the respective ports of the ATM so that data can be written to and read from the external memory.

The above argued difference between the claimed device and method vis-à-vis the device and method of Pei undermine the factual determination that Pei identically describes the claimed invention within the meaning of 35 U.S.C. § 102. ***Minnesota Mining & Manufacturing Co. v. Johnson & Johnson Orthopaedics Inc.,*** 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992); ***Kloster Speedsteel AB v. Crucible Inc.,*** 793 F.2d 1565, 230 USPQ 81 (Fed. Cir. 1986). Applicants, therefore, submit that the imposed rejection of independent claims 1 and 11, and dependent claims 2 and 4, under 35 U.S.C. §102 for lack of novelty as evidenced by Pei is not

factually or legally viable and, hence, solicit withdrawal thereof. The allowance of claims 1, 2, 4 and 11 is respectfully solicited also.

Claims 3, 6, 8-10, 12, 16-19, 21 and 23-25 are rejected under 35 U.S.C. §103(a) as being unpatentable over Pei et al. as applied to claims 1, 2, 4 and 11 above, and further in view of Daniel et al.

The rejections are respectfully traversed.

Claims 3, 6, 8-10 depend from claim 1 and claims 12 and 16 depend from claim 11. As independent claims 1 and 11 are patentable over Pei, dependent claims 3, 6, 8-10, 12 and 16 are patentable over Pei also, even when considered in vide of Daniel et al.

Amended claim 17 recites, *inter alia*:

> (2) a scheduler for ***selectively assigning memory access slots to respective ports*** based on a selected one of the plurality of programmable system settings stored in the first memory; ...

Thus, independent claim 17 is patentable over Pei for the same reasons as to why independent claims 1 and 11 are patentable over this reference. Similarly, independent claim 17, and claims 18, 19, 21 and 23-25 depending from claim 17, are patentable over Pei and Daniel et al., considered alone or in combination. Therefore, the allowance of claims 3, 6, 8-10, 12, 16-19, 21 and 23-25 is respectfully solicited.

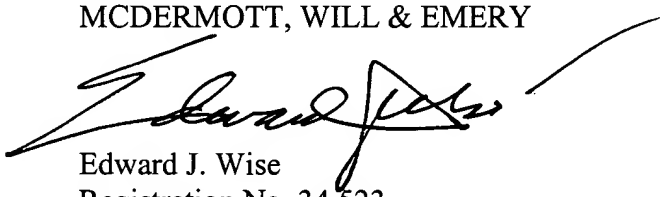
CONCLUSION

Accordingly, it is urged that the application, as now amended, is in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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VERSION WITH MARKINGS SHOWING CHANGES MADE

IN THE CLAIMS

Please amend claims 4, 13, 15, 17, 18, 19 and 21-24 as follows:

4. (Amended) The network switch according to claim 1, wherein each said programmable information entry includes a port operation code, and the scheduler sets the operation of a [the] port based on the port operation code.

13. (Amended) The method according to claim 12, wherein the storing step comprises setting each slot-to-port assignment within the slot-to-port assign configuration to include one of a read and a write bit for indicating whether a [the] corresponding memory access slot is one of a read and write slot.

15. (Amended) The method according to claim 13, [12,] wherein the storing step includes storing into the slot-to-port assignment configuration a wrap-around bit that returns the sequence to a first memory access slot at a start of the sequence from an "Nth" memory access slot.

17. (Amended) A switched network system comprising:

a first memory for storing a plurality of programmable system settings;

a second memory for storing data packets;

a network switch having a plurality of ports configured for transferring data packets, the network switch including:

(1) an external memory interface configured for transferring data packets between the network switch and the second memory; and

(2) a scheduler for selectively assigning memory access slots to respective ports based on a selected one of the plurality of programmable system settings stored in the first [assignment table] memory; and

a system controller for supplying the selected one of the plurality of programmable system settings to the network switch.

18. (Amended) The switched network system according to claim 17, wherein the external memory interface includes a memory access slot assignment table memory.

19. (Amended) The switched network system according to claim 17, wherein the plurality of programmable [information includes] system settings include a port operation code, and the scheduler sets the operation of the port based on the port operation code.

21. (Amended) The switched network system according to claim 17, wherein the plurality of programmable [information includes] system settings include a sequence of an N number of memory access slot assignments that is continuously repeated by the scheduler in assigning memory access slots.

22. (Amended) The switched network system according to claim 21, wherein the plurality of programmable [information includes] system settings include a wrap-around bit at an end of the sequence and the scheduler returns to a first memory access slot at a start of the sequence upon detecting the wrap-around bit.

23. (Amended) The switched network system according to claim 18, wherein the memory access slot assignment table memory is a RAM.

24. (Amended) The switched network system according to claim 18, wherein the memory access slot assignment table memory is a group of registers.